Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A processor comprising:

first and second instruction pointer (IP) sources to provide IPs for first and second instruction threads, respectively;

an instruction cache to provide a cache line responsive to an IP;

a source arbiter to provide an IP from the first or second IP source to the instruction cache;

an instruction buffer (IB) to receive a first block of the cache line from the instruction cache; and

a temporary instruction cache (TIC) to receive a second block of the cache line in the same clock cycle, the IB and the TIC receive the first and second blocks of the cache line on a first clock interval, wherein the second block of the cache line is transferred to the IB on a subsequent clock interval, the source arbiter provides IPs from the first and second sources on alternate clock intervals, wherein the IB includes first and second IBs to store instructions from the first and second threads, respectively, and wherein the first IB receives an instruction block from the TIC and the second IB receives an instruction block from the cache on a second clock interval.

Claims 2-8 (cancelled)

Claim 9 (currently amended): A processor comprising:

first and second instruction pointer (IP) sources to provide IPs for first and second instruction threads, respectively;

an instruction cache to provide a cache line responsive to an IP;

a source arbiter to provide an IP from the first or second IP source to the instruction cache;

an instruction buffer (IB) to receive a first block of the cache line from the instruction cache; and

a temporary instruction cache (TIC) to receive a second block of the cache line in the same clock cycle, wherein the IB comprises first and second IBs and the instruction cache provides instruction blocks to the first and second IBs on adjacent clock cycles, wherein the TIC provides instruction blocks to the first and second IBs on subsequent adjacent clock cycles.

Claim 10 (currently amended): An instruction fetch engine comprising:

an instruction cache to provide a line of instructions in response to an instruction pointer;

an instruction queue to receive a first block of the instruction line from the instruction cache during a first clock interval; and

a temporary instruction cache to receive a second block of the instruction line during the first clock interval, wherein the instruction cache stores lines of instructions for first and second instruction threads and the instruction queue includes first and second instruction queues to store blocks of instructions for the first and second instruction threads, respectively, wherein the instruction cache provides first and second blocks of a line of instructions for the first instruction thread to the first instruction queue and the temporary instruction cache, respectively, during the first clock interval, wherein the instruction cache provides first and second blocks of a line of instructions for the second instruction thread to the second instruction queue and the temporary instruction cache, respectively, during a second clock interval.

Claims 11-15 (cancelled)

Claim 16 (currently amended): An instruction fetch engine comprising:

an instruction cache to provide a line of instructions in response to an instruction pointer;

an instruction queue to receive a first block of the instruction line during a first clock interval; and

a temporary instruction cache to receive a second block of the instruction line during the first clock interval, wherein the instruction queue includes first and second instruction queues and the instruction cache provides first blocks of instruction lines for the first and second instruction threads to the first and second instruction queues on alternate clock intervals, wherein the instruction queue provides second blocks of the

instruction lines for the first and second instruction threads to the temporary instruction cache on subsequent alternate clock intervals.

Claim 17 (original): The instruction fetch engine of claim 16, wherein the temporary instruction cache provides the second blocks of the instruction lines for the first and second instruction threads to the first and second instruction queues, respectively, on alternate clock intervals.

Claim 18 (currently amended): A method comprising:

selecting first and second cache lines for first and second instruction threads;

providing first and second instruction blocks of the first cache line to a first instruction queue and a temporary instruction cache, respectively, during a first clock interval;

providing first and second instruction blocks of the second cache line to a second instruction queue and the temporary instruction cache, respectively, during a second clock interval, and

providing the second block of the first cache line from the temporary instruction cache to the first instruction queue during the second clock interval.

Claim 19 (cancelled)

Claim 20 (previously presented): The method of claim 18, wherein selecting first and second cache lines comprises:

receiving instruction pointers for the first and second threads; and

providing first and second cache lines responsive to receipt of the instruction pointers for the first and second threads, respectively.

Claim 21 (original): The method of claim 20, wherein receiving instruction pointers for the first and second threads comprises receiving instruction pointers for the first and second threads during adjacent clock intervals.

Claim 22 (original): The method of claim 21, wherein providing the first and second instruction blocks comprises providing the first and second instruction blocks during adjacent clock intervals.

Claims 23-26 (cancelled)